

EE788: Advanced CMOS Logic and Flash Memory Devices : Mini-Project - Gate Tunneling Currents

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General Info

(A) The paper by Register (1999, APL) provides a formulation of tunnelling leakage via gate oxide, where leakage current density is calculated as a function of oxide field, using a simple WKB (with reflection) approach.

(B) The paper by Wu (2006, SSE) provides a simple approach (numerical solution for Schrodinger - Poisson in the substrate) that can be used to calculate the relation between gate voltage and oxide field, and uses WKB for leakage current.

(C) The paper by Ando (2011, EDL) provides a formulation of leakage via HKMG (IL/High-K dual layer gate insulator) stack.

Instructions

(1) Obtain gate voltage versus surface band bending using Schrodinger - Poisson (as in (A)) and only Poisson (as done in class). Use $T_{ox} = 1.5\text{nm}$ and 3nm .

(2) Calculate leakage current versus gate voltage, using Schrodinger - Poisson and only Poisson for substrate electrostatics. Do this without and with the reflection term used in (B). Use $T_{ox} = 1.5\text{nm}$ and 3nm .

(3) In (B), the tunnelling integral (in energy) is approximated. What happens if you remove the approximation and execute the integral? Use $T_{ox} = 1.5\text{nm}$ and 3nm .

(4) Develop a formulation for HKMG stack (using (A) and (B), suitably modifying for bi-layer) and compare with data shown in (C).

Use surface potential (as in (B)) to calculate the field and use (A) for tunnelling leakage. Addition: Validate (2) using Fig.6 data (use a snipping tool to grab) of the attached paper.

Gate Bulk vs Surface Potential – Part 1

Methods

For Schrodinger Poisson we solve the below equations 1 and 2 self-consistently:

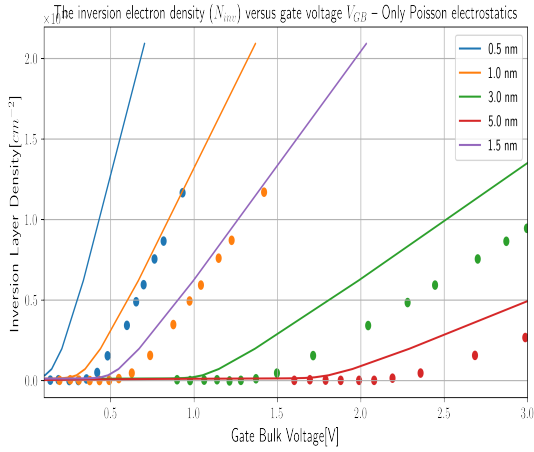
$$\frac{d^2\psi_{ij}(y)}{dy^2} + \frac{2m_{yj}}{\hbar^2} [E_{ij} + q\phi(y)] \psi_{ij}(y) = 0 \quad (1)$$

$$\frac{d^2\phi(y)}{dy^2} = \frac{-q}{\epsilon_{si}} [N_A^-(y) + n(y) - p(y)] \quad (2)$$

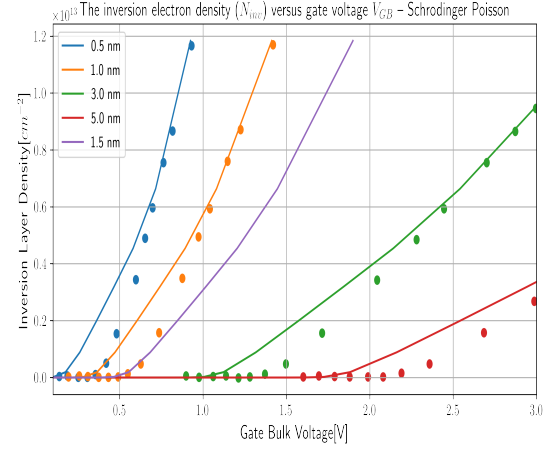
For the only poisson case we solve 2 only. The given datapoints from plot in [2] were used to validate.

Plots

The Inversion charge density plots for the Both simulations are plotted below.

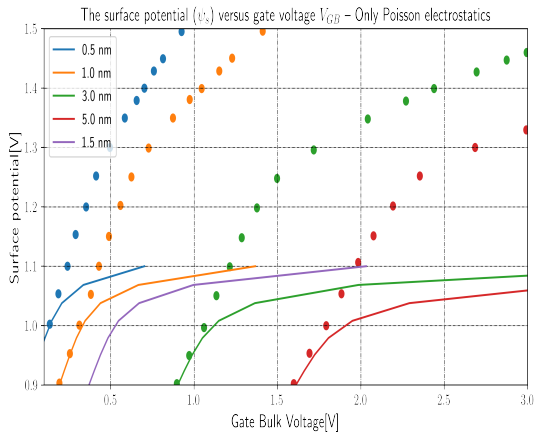


Only Poisson solved Inversion charge density

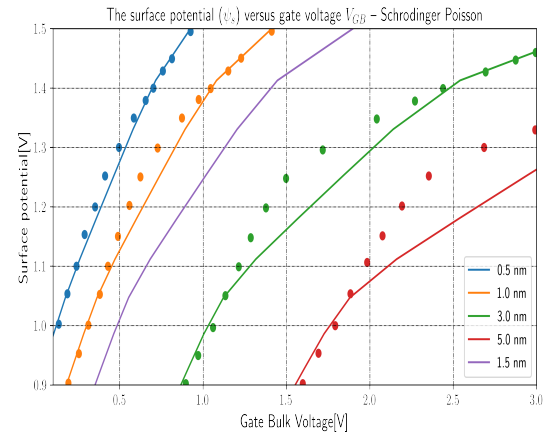


Schrodinger-Poisson solved Inversion charge density

The Gate Bulk Voltage vs the Surface Potential for the Both simulations are plotted below.



Only Poisson solved ψ_s vs V_{GB}



Schrodinger-Poisson solved ψ_s vs V_{GB}

Inferences

Here on solving as described in [2] we get good match with the datapoints than that of only poisson case. In *only poisson* case, we see high values of inversion charges at considerable lower voltages as it considers the charges continuous over energy space. However, at high inversion like as depicted in the figures, quantization of charges occur in discrete energy levels possible. Hence the growth of charge with voltage is slower and requires more applied voltage than the poisson case to reach high charge density. It is also mentionable that we get similar profile for both *Schrodinger-poisson* and *Poisson* solutions in depletion and weak inversion regimes.

Besides we also note large V_{gb} for considerably lower ψ_S owing to the same reason of generation of very high inversion charge carrier density in *Poisson case*.

Gate Bulk vs Tunneling Leakage – Sub-Part 2

Methods

We use WKB approximation from [1] for all calculations shown here. Some relevant equations were:

$$T_{\text{WKB}} = \exp \left[\frac{E_g \sqrt{2m_{\text{ox}}}}{4\hbar q F_{\text{ox}}} (2\gamma' \sqrt{\gamma} + \sqrt{E_g} \sin^{-1} \gamma') \right] \Big|_{E_{\text{ox}}=q\phi_{\text{an}}}^{E_{\text{ox}}=q\phi_{\text{cat}}} \quad (3)$$

$$Q = \epsilon_{\text{ox}} F_{\text{ox}} \quad (4)$$

$$f = 0.6 \times \frac{2q}{(3\pi\hbar q m_{\text{si},\perp})^{1/3}} \left(\frac{\epsilon_{\text{ox}} F_{\text{ox}}}{\epsilon_{\text{si}}} \right)^{2/3} \quad (5)$$

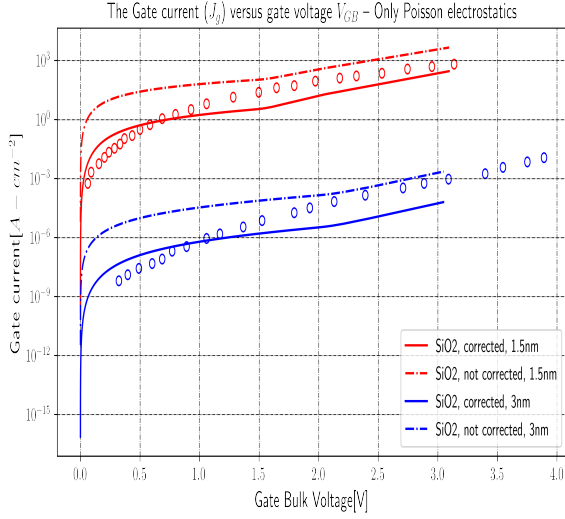
$$T_{\text{R}} = \frac{4v_{\text{si},\perp}(E_{\text{si},\perp}) \nu_{\text{ox}}(q\phi_{\text{cat}})}{v_{\text{si},\perp}^2(E_{\text{si},\perp}) + \nu_{\text{ox}}^2(q\phi_{\text{cat}})} \times \frac{4v_{\text{si},\perp}(E_{\text{si},\perp} + qF_{\text{ox}}t_{\text{ox}}) \nu_{\text{ox}}(q\phi_{\text{an}})}{v_{\text{si},\perp}^2(E_{\text{si},\perp} + qF_{\text{ox}}t_{\text{ox}}) + \nu_{\text{ox}}^2(q\phi_{\text{an}})} \quad (6)$$

$$J_g = \frac{\eta q m_{\text{si},U} f}{\pi \hbar^2} \int_0^{E_{\text{F}} - E_{\text{si},\perp}} T dE_{\text{si},1} \simeq Q f T \Big|_{E_{\text{si},1}=1/2(E_{\text{F}} - E_{\text{si},1})} \quad (7)$$

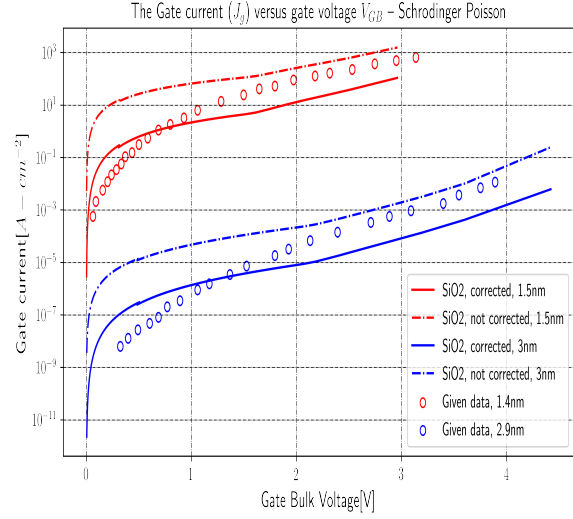
Both Reflection corrected(Include effect of 6) and uncorrected version are plotted in the same curve.

Plots

The gate tunneling leakage current vs gate to bulk voltage are plotted below.



Only Poisson solved Gate leakage current



Schrodinger-Poisson solved Gate leakage current

Inferences

We see higher tunneling currents for the version which doesn't account for reflection as might be seen from the physical picture. We are plotting everything in the Direct tunneling regime and hence only those parts are compared to give satisfactory match. Roll-off is also seen at lower V_g owing to low electric field in oxide due to low carrier density.

Integral Form of Leakage Current – Sub-Part 3

Methods

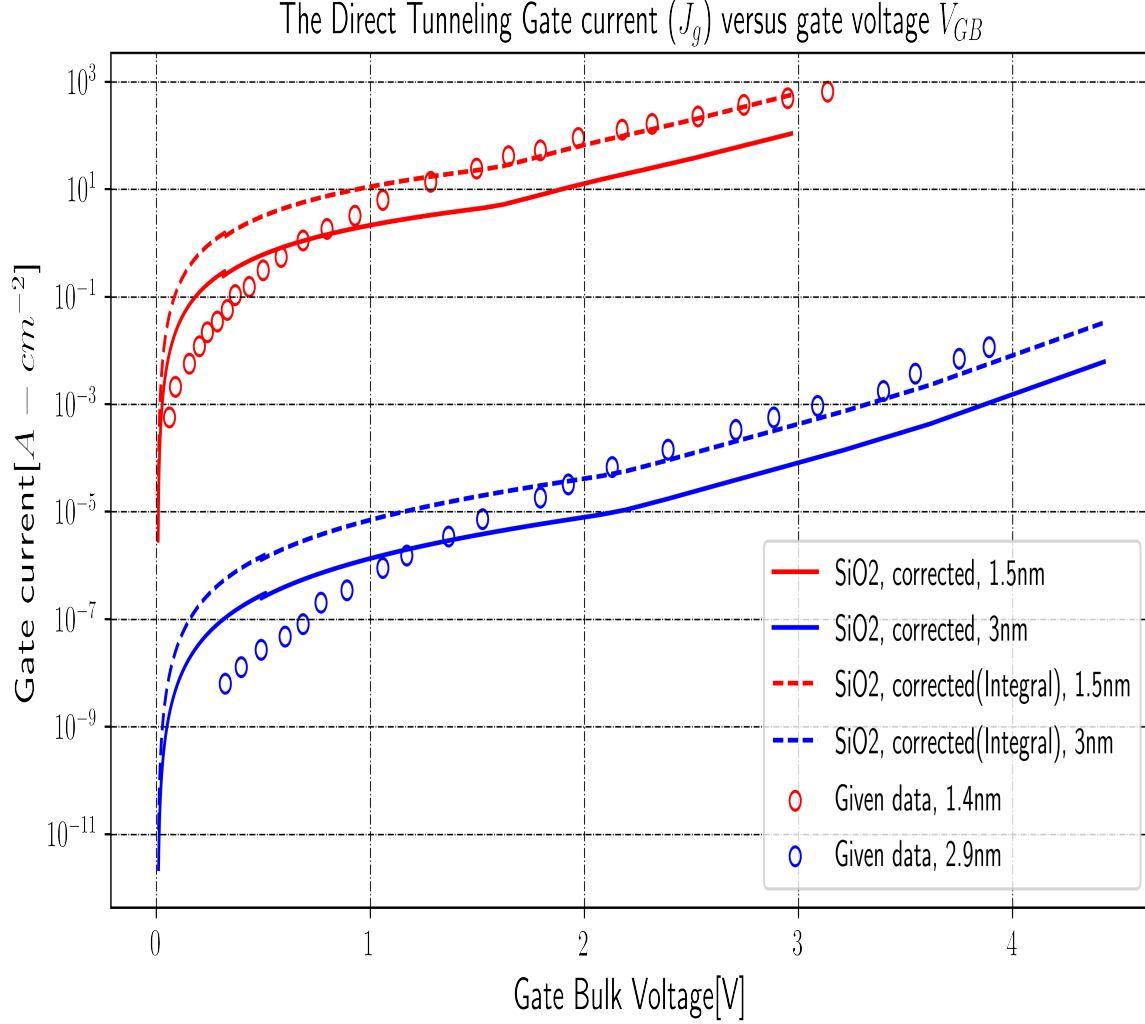
Instead of approximation in equation 7 we use the integral over energy following the below expression :

$$J_g = \frac{\eta q m_{\text{si},\parallel} f}{\pi \hbar^2} \int_0^{E_F - E_{\text{si},\perp}} T dE_{\text{si},\parallel} \quad (8)$$

We only proceed with Schrodinger-Poisson version of (Eqn 2 and 1) from this method onwards.

Plots

The relevant plots for $t_{\text{ox}} = 1.5\text{nm}$ and 3nm are shown on next page.



Results of using Integral form vs Approximate form of WKB tunneling leakage current

Inference

On the integral, we find the reason for taking approximation from the paper as: *A midpoint approximation to the integral is used for simplicity to obtain the mean tunneling probability while introducing very little error.* The integral version however seems to give a little bit higher value of current than the mean value. For higher V_{gb} values the match with datapoints extracted seem better while the approximation fares better at lower V_{gb} values. Hence the variation of distribution of the parameter $E_{si||}$ may not be uniform resulting in the errors.

Leakage Current in Bilayer Stack – Sub-Part 4

Methods

The Idea implemented is discussed in [5]. The relevant Equations were modified from ref [1] and [2] taking into account the changed factors for bilayer stack. Some figures to give idea of the problem is included below:

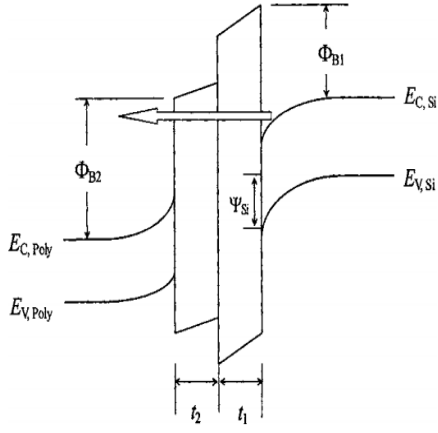


FIG. 2. Illustration of band diagram for dual-layer gate dielectric films with $\Phi_1 > \Phi_2$.

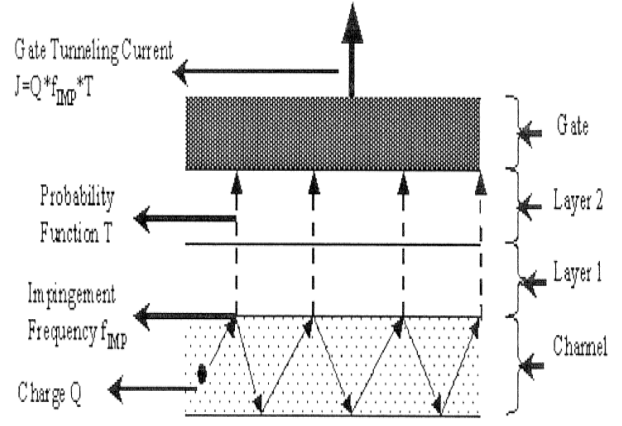


Figure 1: Components of tunneling current.

- We use 5 and 4 to get the Impinge frequency f and total carrier concentration available for tunneling Q . It is noteworthy that both have same values in both the stacks as modeled in [1] and [6].
- Next we use the following from [5]: *For multiple-layer dielectric film, supposing that the direct tunneling occurs at all layers, the overall tunneling probability is given by the multiplying rule,*

$$T = T_1 T_2 \cdots T_M \quad (9)$$

where T_1, T_2 , and T_M are the tunneling probability for first layer, second layer, and M th layer, respectively.

- The tunneling probabilities can be obtained thus by multiplying the tunneling coefficients of both layers. An approximate version is given below,

$$J_{DT} \approx J_0 \left(1 - \frac{1}{2} V_1 / \Phi_{B1} \right) \left(1 - \frac{1}{2} V_2 / \Phi_{B2} \right) \times \exp [-2\beta (\alpha_1 - \alpha_1 V_1 / 4\Phi_{B1} + \alpha_2 - \alpha_2 V_2 / 4\Phi_{B2})] \quad (10)$$

We however use the full version, as in 7 for the plots depicted below to get better accuracy.

- The relationship between the two potentials is governed by Gauss's law for voltage dividing [5], i.e.,

$$\frac{\kappa_1 V_1}{t_1} = \frac{\kappa_2 V_2}{t_2} \quad (11)$$

- We use the below tables from [3] as reference for material parameters,

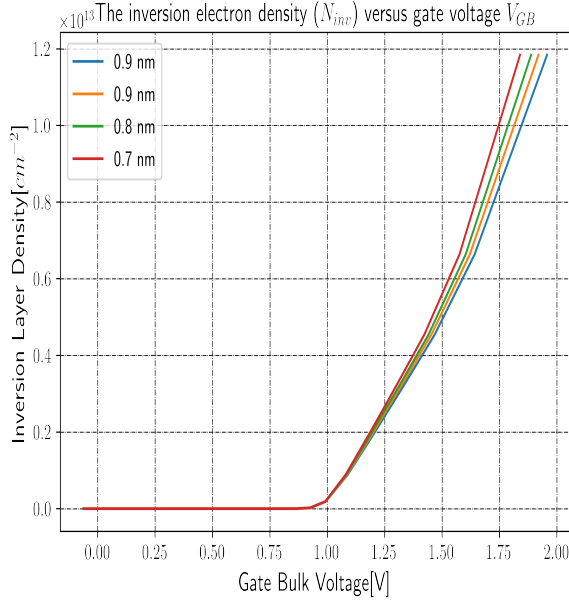
	IL-1-4	IL-5
m_e (SiO ₂)	$0.63m_0$	
m_e (HfO ₂)	$0.25m_0$	
Φ_C (SiO ₂)	3.50eV	3.00eV
Φ_C (HfO ₂)	1.50eV	1.35eV

(12)

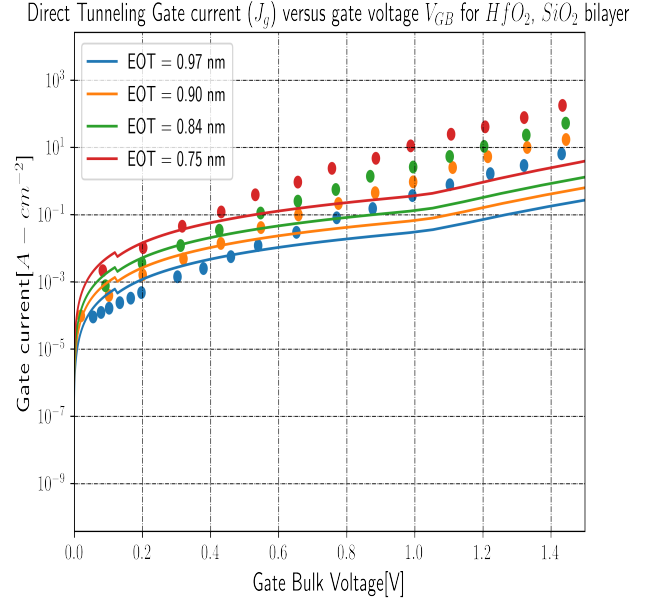
	EOT (Å)	HfO ₂ thickness (Å)	IL thickness (Å) (*)	nFET V_t (V)	pFET V_t (V)
IL-1	9.7	22	5.4	0.40	-0.77
IL-2	9.0	22	4.7	0.40	
IL-3	8.4	22	4.1	0.41	-0.85
IL-4	7.5	22	3.2	0.40	
IL-5	6.1	22	1.9	0.40	-0.81

Plots

We plot for the IL layers as given below,



Inversion Charge vs Gate Bulk Voltages for IL 1-4 Bilayer Stack



Tunneling currents for IL 1-4 Bilayer Stack

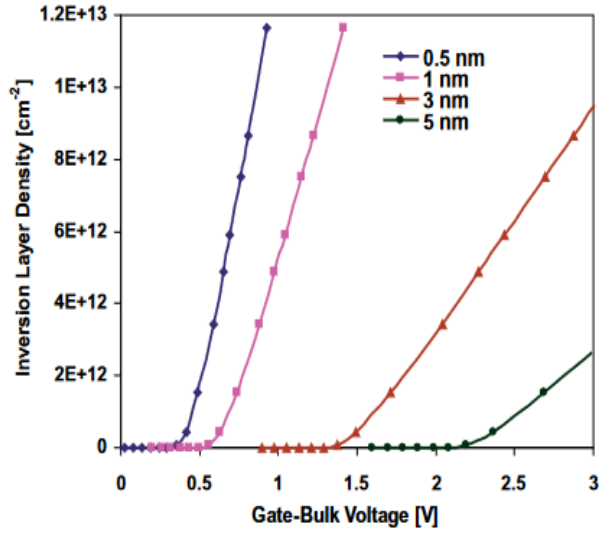
Inferences

The datapoints obtained in [3] are found by finite modelling of devices. So they are supposedly more accurate than the crude approximation of double barrier we have taken. Although the slope of the curves obtained are similar, macroscopic approximations involved in the model seems to work at lower V_g values. Some adjustments in V_t was required to get reasonable values.

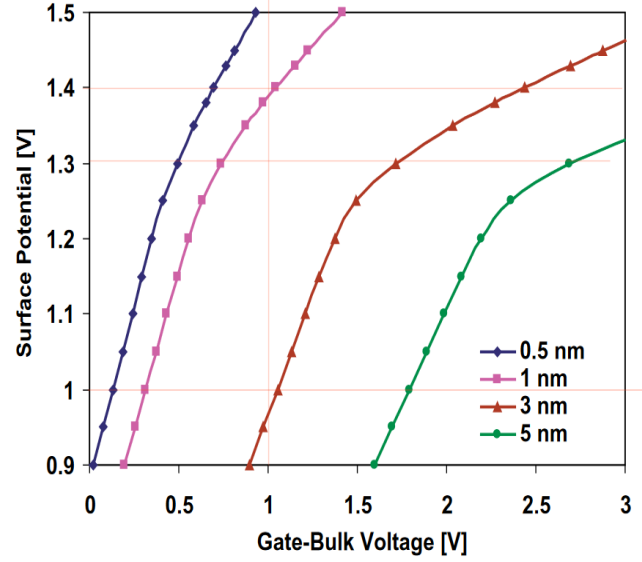
Appendices

Screenshots used to find reference data-points

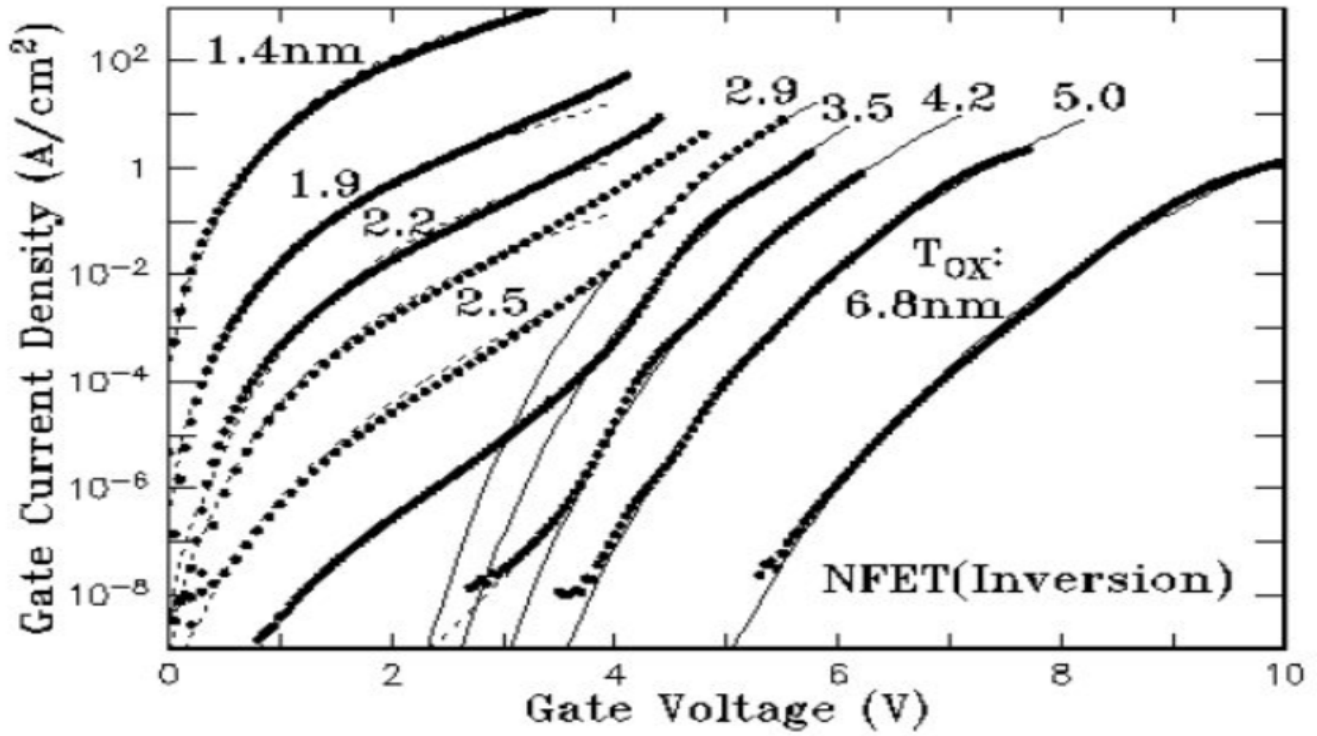
The datapoints were extracted from plots using a webApp, at <https://plotdigitizer.com/app>



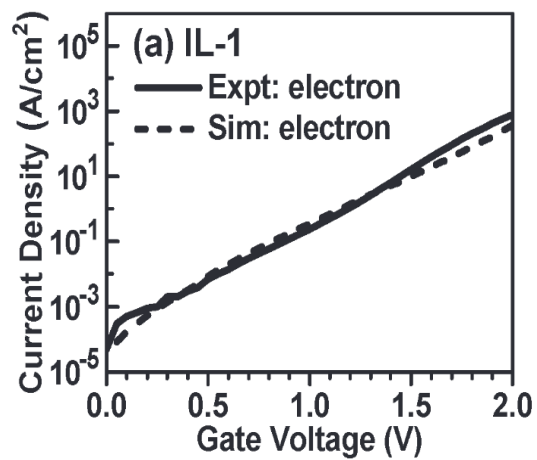
N_{inv} vs V_{gb} from [2]



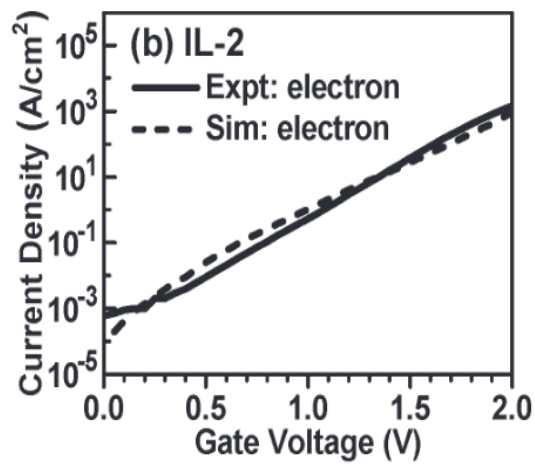
ψ_s vs V_{gb} from [2]



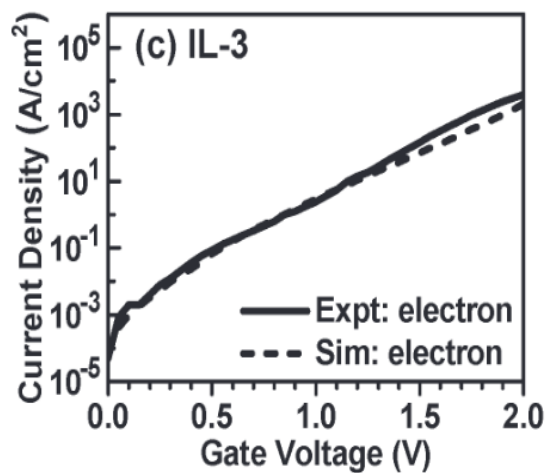
Gate Oxide leakage from [4]



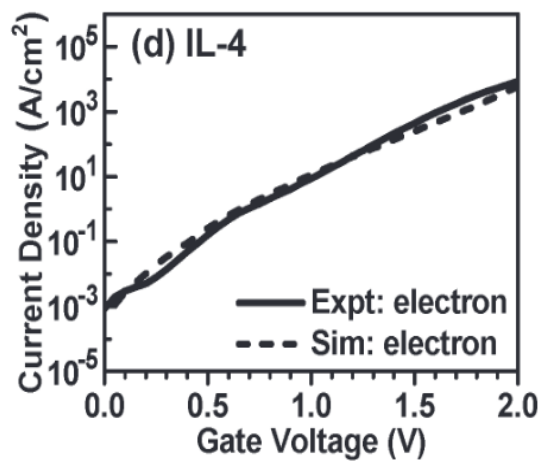
IL-1 from [3]



IL-1 from [3]



IL-1 from [3]



IL-1 from [3]

Bibliography

- [1] Leonard F. Register, Elyse Rosenbaum, and Kevin Yang, Analytic model for direct tunneling current in polycrystalline silicon-gate metal–oxide– semiconductor devices, *Appl. Phys. Lett.*, 74, 457 (1999)
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- [3] Ando et al.: On the Electron and Hole Tunneling in a HfO₂ Gate Stack With Extreme Interfacial-Layer Scaling *IEEE Electron Device Lett.* 12:524.
- [4] Ernest Y. Wu, Jordi Suñé¹, and Rolf-Peter Vollertsen², Comprehensive physics-based breakdown model for reliability assessment of oxides with thickness ranging from 1 nm up to 12 nm, *IEEE CFP09RPS-CDR 47th Annual International Reliability*, 2009
- [5] Hei Wong and Hiroshi Iwai, Modeling and characterization of direct-tunneling current in dual-layer ultrathin-gate dielectric films, *Journal of Vacuum Science Technology B: Microelectronics and Nanometer Structures Processing, Measurement and Phenomena*, 24, 1785 (2006); doi: 10.1116/1.2213268
- [6] Dunga et al, Modeling of Direct Tunneling Current in Multi-layer Gate Stacks, *Nanotech 2003, Vol. 2*, *www.nsti.org*, ISBN 0-9728422-1-7