Clap detector for toy and appliance control

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Abstract

This project is aimed at designing a circuit that will detect the occurence of a clap and depending on the interval between the claps, provide a visual feedback to the user. For a single voltage supply of 5 V provided to us, one of the objectives is to design a pre-amplifier for an electret microphone used as input. Then one can design a circuit based on uniqueness of the clap waveform envelope that will generate a pulse when a clap input is detected. Finally, we devise control codes for a microcontroller to provide visual feedback to the user, depending on the interval between two successive claps.

Contents

1 Block Diagram of the circuit

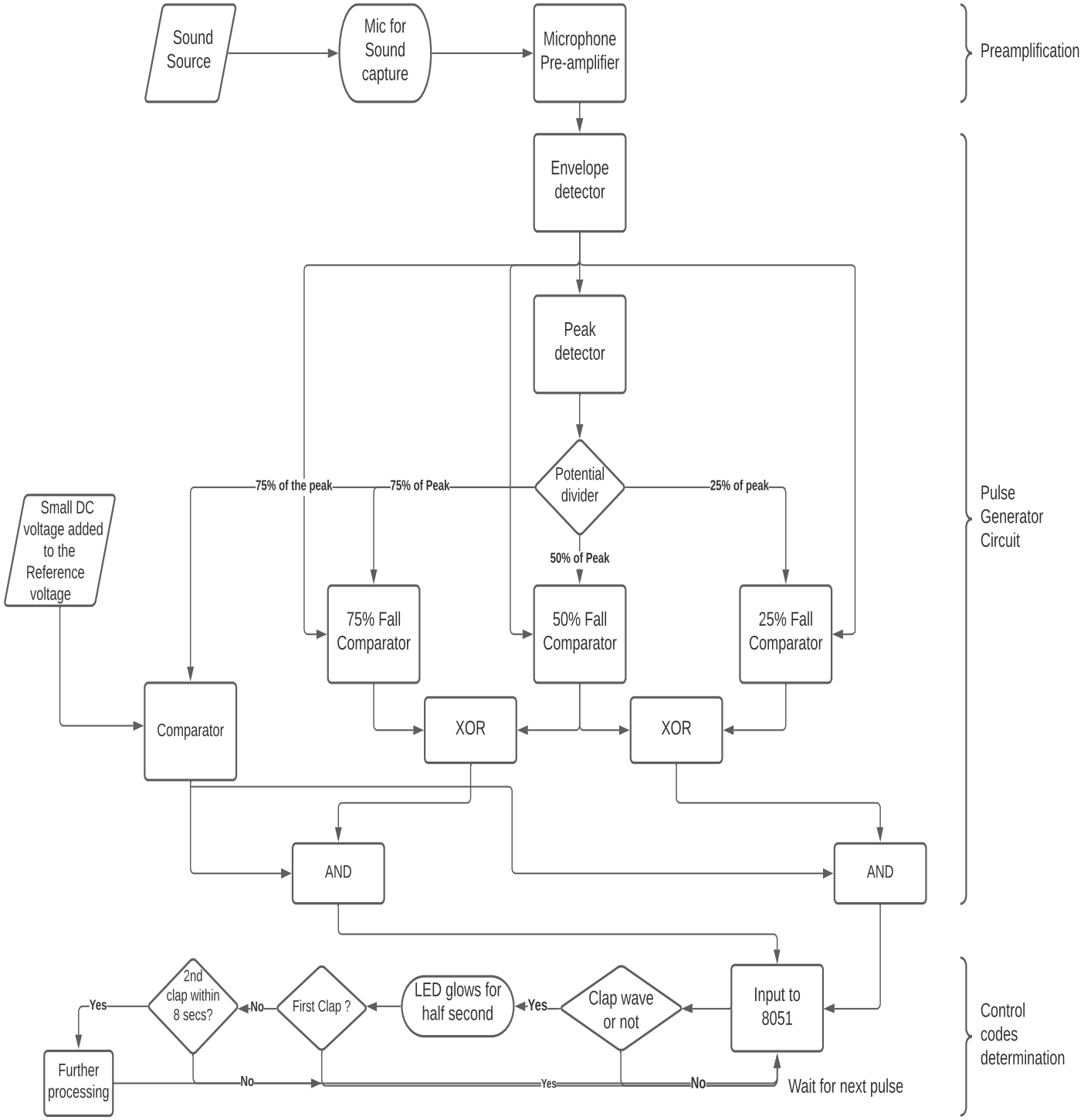

Figure 1: Block diagram with subparts and logic flow

2 A brief description of our design approach

We had initially collected data on the fall times of various waveforms like clap, tap on the table. Also, we looked into the working of the electret microphone [1] and from [3], learnt how to interpret the datasheet

of the microphone [2] that would be used in this project. This was essential in working out the DC voltage level as well as the swing in the current waveform that is sunk into the microphone.

As a single power supply of 5 V was provided to us, we looked into the datasheet for the Op-Amp [5] to be used to work out the maximum allowed swing and the DC voltage level. In the single supply configuration, the input and the output voltage swings from 0 V to $V_{cc} - 1.5 = 3.5$ V and we have decided to limit the swing to 3 V for safety reasons. A DC bias of 1.5 V is then required to allow the input as well as the output to have a symmetrical swing of 1.5 V about the DC bias, something that will be done by the reference generator to be discussed in a greater detail in a later section.

As the microphone output is a current signal, it makes sense to use a trans-impedance amplifier for current-to-voltage conversion as subsequent blocks make use of voltage signals. Given the allowed swing in the output voltage and the input current of the amplifier, the trans-resistance is computed and in addition to this, the value of the DC blocking capacitor is chosen in a manner such that the cutoff frequency is brought as low as possible.

The voltage signal from the pre-amplifier is sent to an envelope detector designed using precision rectifiers [6] to counteract the voltage drop by having only a diode in the circuit. The envelope detector output is sent to a peak detector which holds 75%, 50% and 25% of the peak value. A system of comparators followed by XOR gates are used to obtain pulses corresponding to the duration in which the envelope of the waveform drops from 75% to 50% and 50% to 25%. Outputs of these XOR gates are sent to microcontroller only when the peak detected is greater than a certain threshold. These pulses are then fed into an 8051 microcontroller which, depending on the duration of these pulses determines whether a clap waveform has been detected or not. If at all a clap has been detected, the microcontroller waits for the next set of pulses to determine if a second clap has been registered within a certain time limit so that it distinguishes between two claps done far apart and two claps in quick succession.

3 Detailed design procedure of various subsystems

3.1 Reference Generator

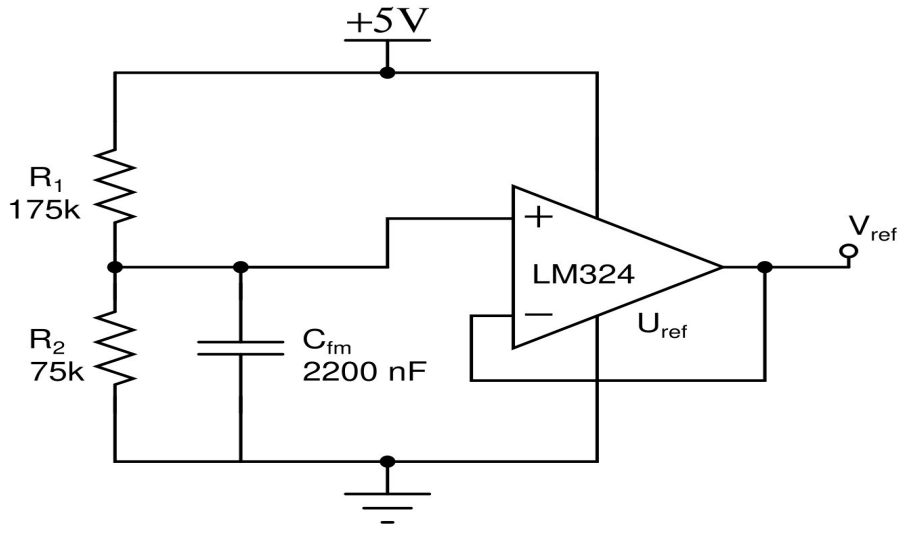

Figure 2: Schematic of Reference Generator

In all circuits that are deployed in this project, the Op-Amps used are LM324 and given that a single power supply of 5 V is provided to us, the range of input and output voltages that can be applied to, or delivered by LM324 goes all the way from 0 to 3.5 V ($V_{cc} - 1.5$ as per [5]). We shall limit our voltage swing on the input as well as the output of the Op-Amps to 3 V for safety reasons, which would imply that a symmetrical swing of 1.5 V is allowed if we worked with a bias of 1.5 V. Therefore, a DC bias of 1.5 V is generated using the circuit given in figure 2.

3.2 Electret Microphone with Pre-Amplifier

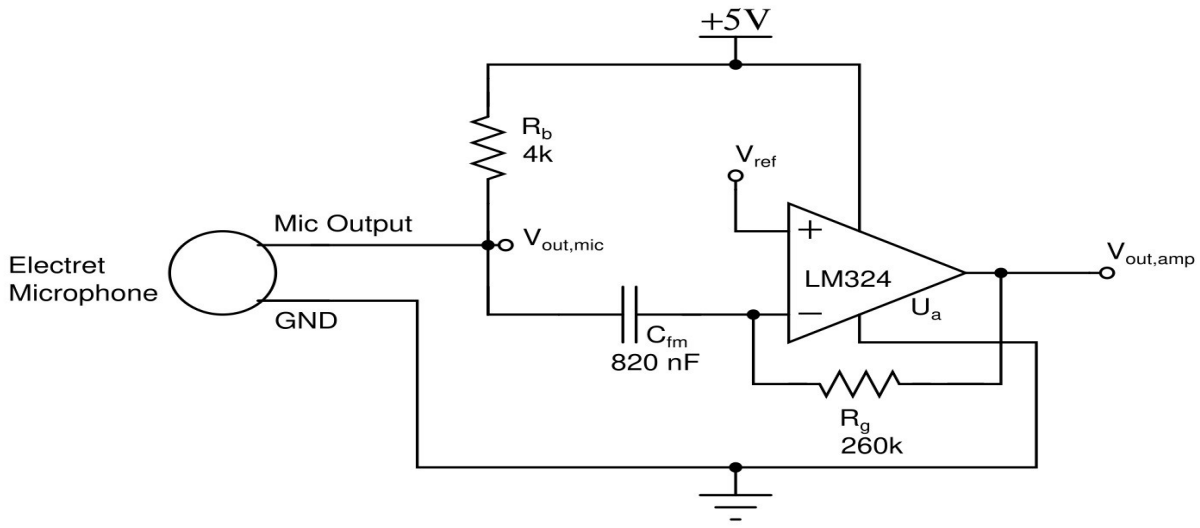

Figure 3: Schematic of Pre-Amplifier for Electret Microphone

3.2.1 DC Analysis: Identification of Operating Points

The microphone to be used is CMA-4544PF-W, an electret condenser microphone. According to the datasheet for the microphone [4], if the supply voltage is taken to be $V_s = 3\ V$, the current sunk into it is $I_{DSS} = 0.5\ mA$. In order to maintain this operating point for the given voltage supply, the biasing resistance is computed to be:

$$R_b = \frac{V_{cc} - V_{out,mic}}{I_{DSS}} \tag{1}$$

Which results in $R_b = 4\ k\Omega$. As this is DC analysis, the capacitor is replaced by an open-circuit and as the non-inverting terminal of U_a is connected to the reference generator output, we can easily conclude that the DC voltage level at the U_a inverting terminal and at the output of U_a is 1.5 V.

3.2.2 AC Analysis: Obtaining Gain and Cutoff Frequency

For the operating point of the microphone, if the sensitivity of the microphone is taken to be $S = 6.309\ mV/Pa$, the impedance of the microphone is taken to be $R_L = 2.2\ k\Omega$, and the maximum pressure level is $\Delta P = 2Pa$, the current swing at the microphone output is given by:

$$\Delta i_{out,mic} = \frac{S\Delta P}{R_L} \tag{2}$$

As the microphone output is a current signal, the pre-amplifier to be used is a trans-impedance amplifier. If the resistance R_g is the trans-impedance of this amplifier, then the maximum voltage swing at the

output of U_a is given by:

$$\Delta v_{out,amp} = \frac{R_g S \Delta P}{R_L} \tag{3}$$

As $v_{amp,out}$ is limited to 1.5 V, this gives us $R_g \approx 261\ k\Omega$. We shall take $R_g = 260\ k\Omega$ as this can be easily realised using a series combination of 240 $k\Omega$ and 20 $k\Omega$ which are available as standard components in the market.
Finally, we are aware that the cutoff frequency of the RC filter formed by R_b and C_{fm} is given by:

$$f_c = \frac{1}{2\pi R_b C_{fm}} \tag{4}$$

Setting $f_c = 50\ Hz$, which is close to the lower limit of audibility, we get $C_{fm} = 795\ nF$. With the requirement of using standard components at hand, we choose $C_{fm} = 820\ nF$ as this reduces the cutoff frequency of the filter to 48.52 Hz.

3.3 Envelope Detector

The schematic is provided at the end of the section. We shall now explain the operation of the circuit:

1. When $V_{out,amp} = V_{out,env}$, no current flows through $R_{env,1}$, $D_{env,1}$ does not conduct, $D_{env,2}$ conducts, and $V_{env,o1}$ is $V_{out,amp} + 0.7$.
2. Case 1: When $V_{out,amp}$ goes above $V_{out,env}$, $U_{env,1}$ tries to go to positive saturation, but $D_{env,2}$ conducts, and $V_{out,env}$ quickly increases to $V_{out,amp}$.
3. Case 2: When $V_{out,amp}$ goes below $V_{out,env}$, $U_{env,1}$ tries to go to negative saturation, but $D_{env,1}$ conducts, $D_{env,2}$ does not conduct and capacitor discharges through the resistor R_{env}, with time constant $R_{env}C_{env}$. When $V_{out,env}$ tries to go below $V_{out,amp}$, we go to case 1 and $V_{out,env}$ stays at $V_{out,amp}$.

We have taken $3R_{env}C_{env} = 200\ ms$, and used $R_{env} = 68\ k\Omega$ and $C_{env} = 1\ \mu F$ (resulting in $3R_{env}C_{env} = 204\ ms$). $R_{env,1}$ is used to limit the current that flows when $V_{out,env}$ decreases to $V_{out,amp}$, a 10 $k\Omega$ resistor is generally used, and we have used the same.
The test signal used to test the functioning of the block: *2 V_{pp} Sinusoid with DC offset of 1.5V with frequency 50Hz*

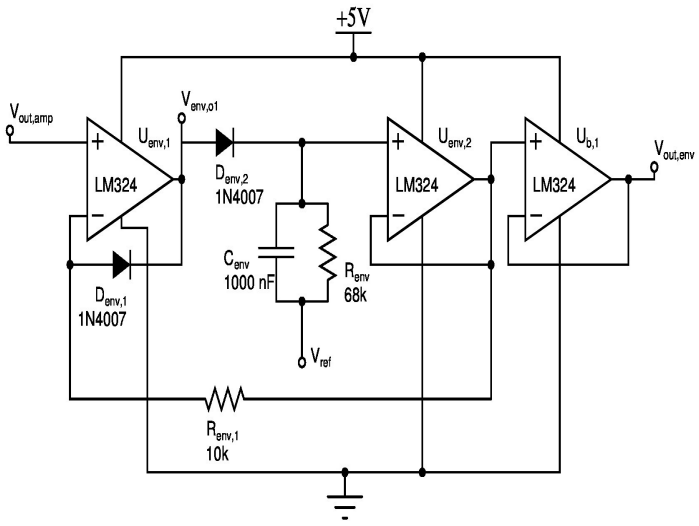

Figure 4: Schematic of Envelope Detector

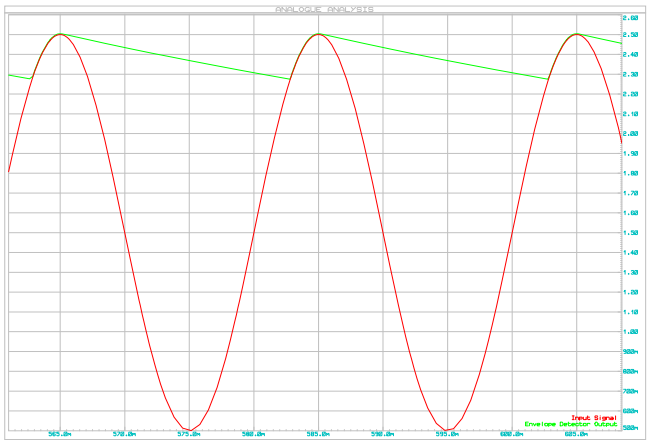

Figure 5: Test input and output from the envelope detector on using DC + Sine Wave

3.4 Peak Detector

The circuit used to hold the peak is similar to the envelope detector, only the values of R_{env} and C_{env} which are R_{pk} and C_{pk} respectively in this case have been changed for larger discharge time. Here we have used $R_{pk} = 510\ k\Omega$ and $C_{pk} = 1\ \mu F$, resulting in $3R_{pk}C_{pk} = 1.53\ s$.
The test signal used to test the functioning of the block: *2 V_{pp} Sinusoid with DC offset of 1.5V with frequency 50Hz*

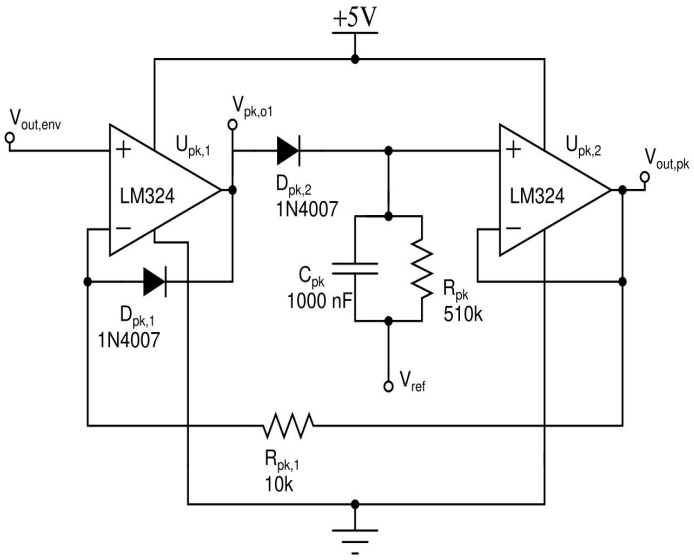

Figure 6: Schematic of Peak Detector

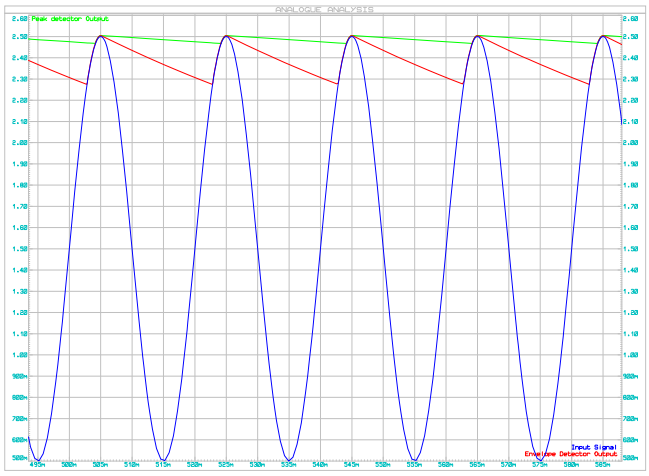

Figure 7: Peak Detector Test input and output

3.5 Comparator Block

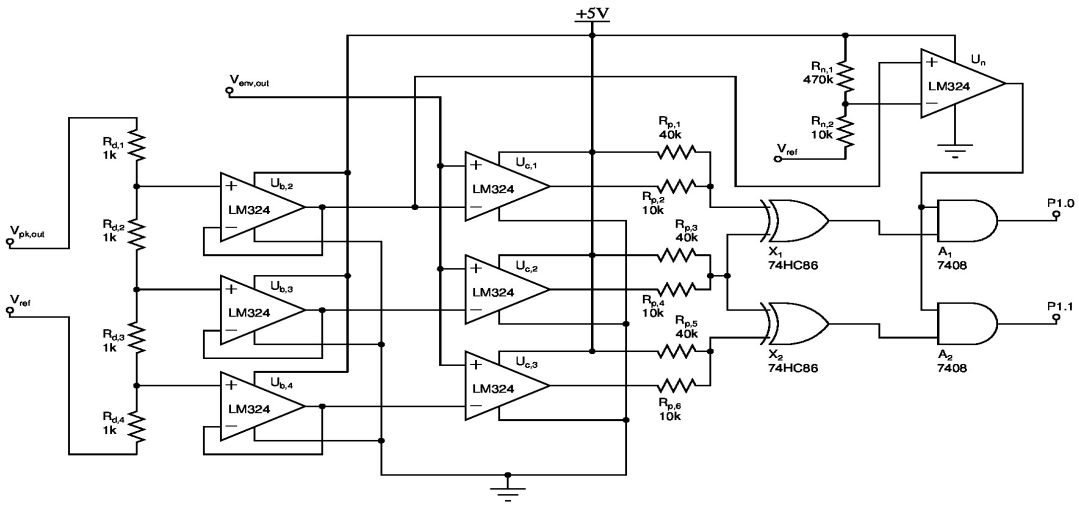

Figure 8: Schematic of Comparator Block

The output from the peak detector $V_{out,pk}$ is fed to a voltage divider to obtain 75%, 50% and 25% of the peak value, relative to the reference voltage used. These threshold values and the envelope detector output $V_{out,env}$ are fed into unity gain buffers after which, they are sent to comparators which toggle from the maximum allowed output (3.5 V) to 0 V when the envelope detector output falls below the

corresponding threshold value. The output from the comparators are fed into 74HC86 XOR gates via pull-up resistors. The value of the pull-up resistors were determined from the V_{iL} and V_{iH} values of 74HC86 by referring to the datasheet [7].

Pull-up resistors were essential because the logical high delivered by the comparators is actually 3.5 V, which is below the V_{iH} of the 74HC86. It turns out that for $U_{c,1}$, if the pull-up resistors are taken to be $R_{p,1} = 40\ k\Omega$ and $R_{p,2} = 10\ k\Omega$, then, assuming that the input current to the XOR gate is negligible, the resistive network essentially behaves like a voltage divider and as a result, the comparator logical high output 3.5 V maps to $3.8V$ and the comparator logical low output 0 V maps to 1 V on the input to the XOR gate. The comparator logical high is mapped to a voltage above the V_{iH} and the comparator logical low is mapped to a voltage below the V_{iL} of the 74HC86 which is what we would require for a proper functioning of the XOR gates. If we now consider the logical high output of the comparator, the current flowing through the pull-up resistors evaluates to 30 μA. The datasheet also suggests that the maximum current taken up by the XOR gate for any input is 1 μA which implies that the voltage divider approximation of the resistive network is a valid one.

Then the XOR gate outputs are fed into AND gates A_1 and A_2, with the other input to the AND gates being the output of comparator U_n, that checks whether the peak detected by the peak detector is above a certain threshold or not. This is done to reduce the false positives encountered due to other disturbances of smaller amplitude when using XOR outputs as input to microcontroller. While the logical high and low levels of the comparator are the same as what we had worked out earlier, we can see that this time, the high level is more than the V_{iH} and the low level is less than the V_{iL} of the 7408 [8] and so, no pull-up resistors are required for this part. The outputs of A_1 and A_2 are fed into the port pins P1.0 and P1.1 of the 8051 microcontroller respectively.

4 Test/simulations results with recorded sound signals

In the PROSPICE simulations, we used the recorded sound clips to generate the pulses using the pulse detector circuit. The input test waveform and consequent output of the envelope detector is shown below.

4.1 Plot of input, envelope detector and peak detector output waveforms

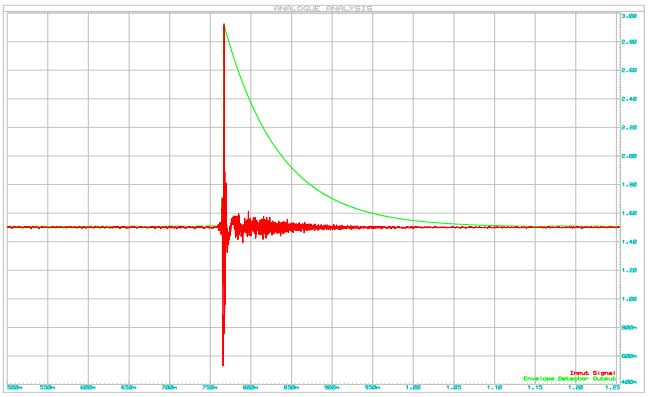

Figure 9: Envelope Detector output with input signal (magnified to show one of the two claps)

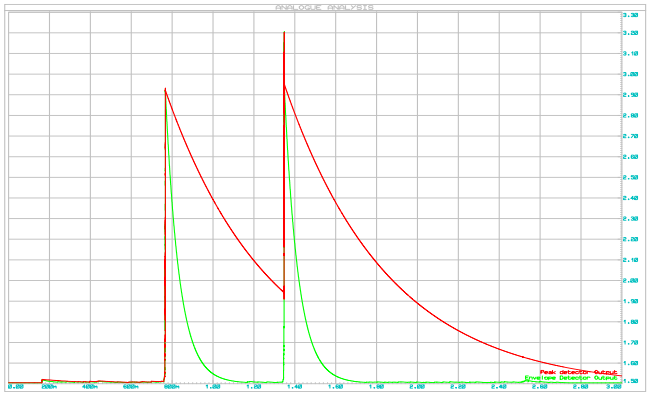

Figure 10: Peak Detector Test input and output

4.2 Plot of threshold voltage and envelope detector output waveforms

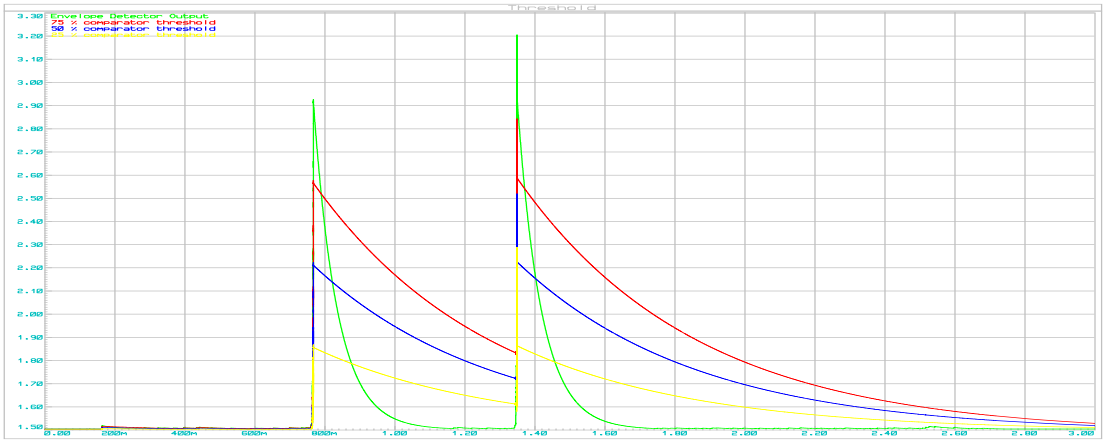

Figure 11: Threshold voltages in the inverting terminal of comparators and envelope detector output

4.3 Pulses obtained before and after applying the AND gates

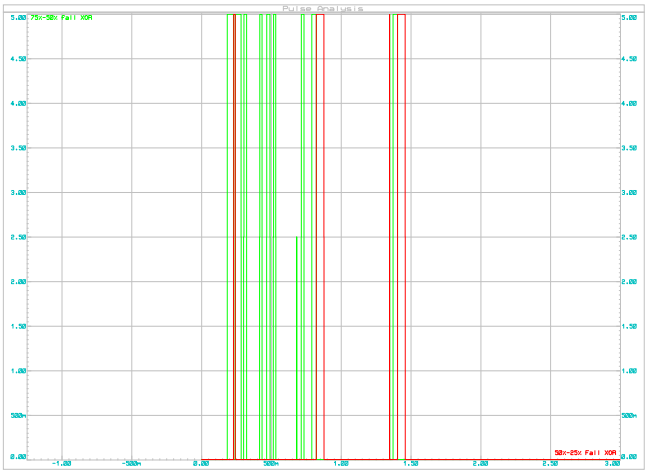

Figure 12: Pulses after the XOR gate

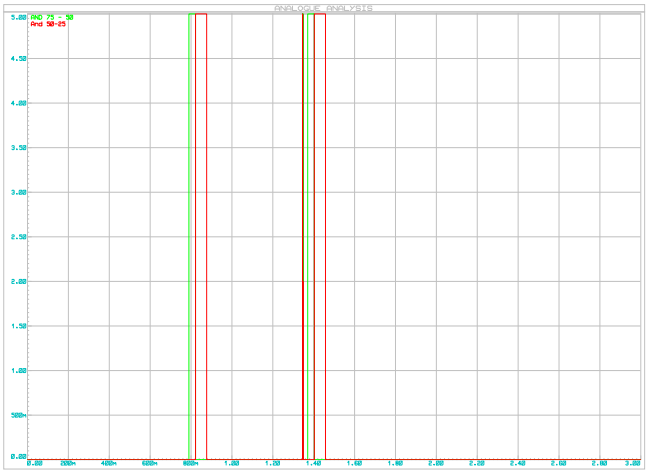

Figure 13: Final pulse after the Comparator U_n and the And gates A_1 and A_2

4.4 Inferences

Certain inferences that can be extracted from the simulations ran,

- The duration of pulse for 75% to 50% fall of envelope have been shown in table 1.
- The duration of pulse for 50% to 25% fall of envelope have been shown in table 1.
- We have decided to take the range for fall times (to be used in control codes) as $[\mu - 3\sigma, \mu + 3\sigma]$ (μ is corresponding mean, σ is corresponding standard deviation).
- The interclap detection time should be at least 1 s, so as to not interfere with generating pulses for one waveform.

Clap number	75% to 50% fall time	50% to 25% fall time
1	32.1 ms	55.4 ms
2	32.1 ms	55 ms
3	32 ms	55 ms
4	33 ms	54 ms
5	32 ms	55 ms
6	32.6 ms	56.1 ms
7	32.1 ms	55 ms
8	33 ms	56 ms
9	32 ms	54.9 ms
mean	32.32 ms	55.15 ms
standard deviation	0.4 ms (0.012* mean)	0.59 ms (0.011* mean)

Table 1: Fall times for different samples of clap

5 Control codes for the 8051 microcontroller

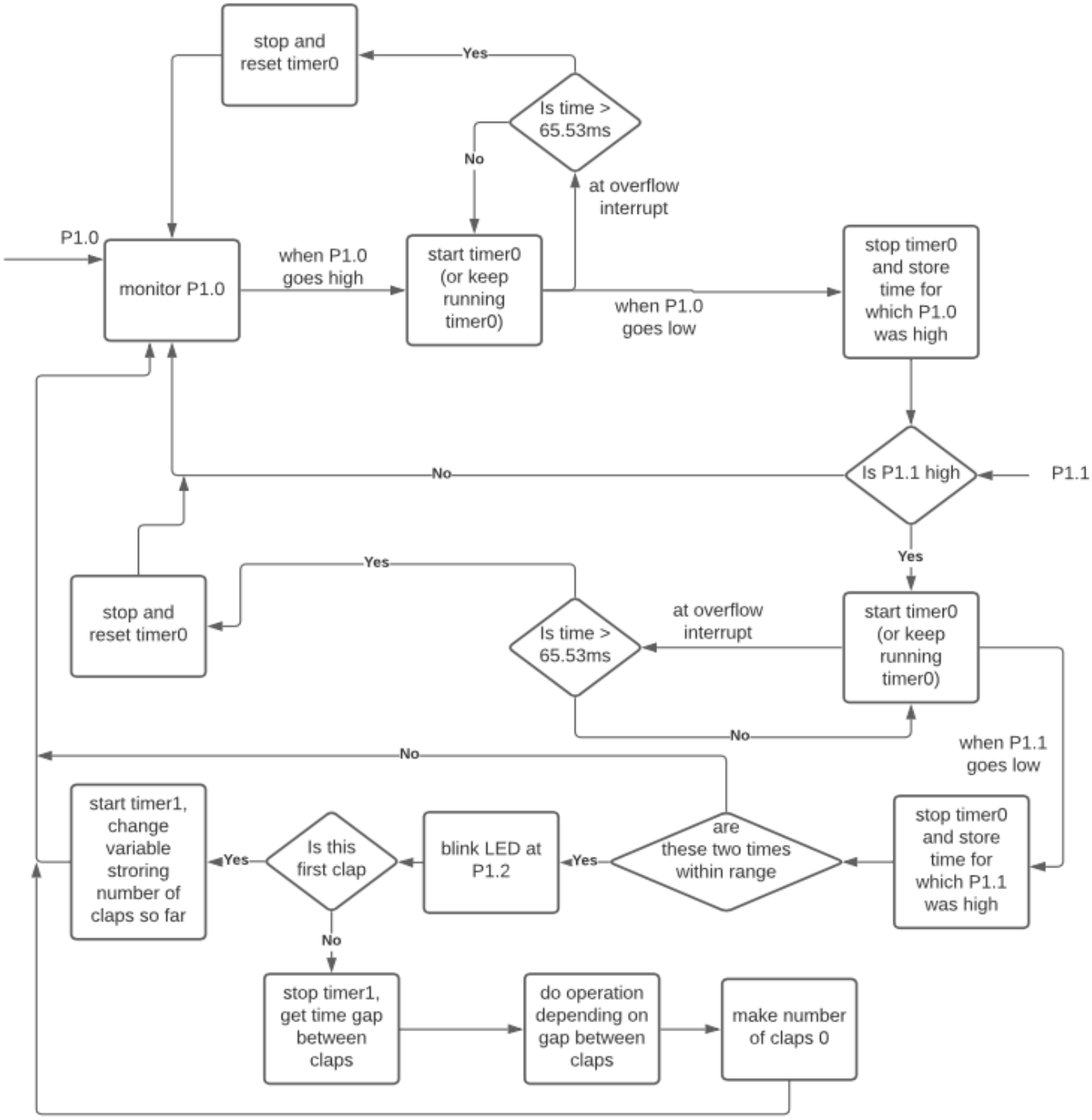

Figure 14: Flow chart explaining control code logic

We have used **Atmel at89c51** controller for programming the control codes. Output of XOR gate corresponding to 75% *to* 50% has been connected to P1.0, and XOR gate corresponding to 50% *to* 25% has been connected to P1.1. We have used an LED connected at P1.2 to convey to the user that a clap has been detected. LEDs connected to P1.4 to P1.7 are supposed to blink depending on the interclap duration as shown in table 2.

As shown in figure 14, microcontroller continuously monitors status of P1.0, whenever P1.0 goes high, it starts timer0 and waits for P1.0 to go low. If P1.0 does not go low within 65.53ms, microcontroller decides this is not a clap, and starts monitoring P1.0 again.
If P1.0 does go to 0 within 65.53ms, the microcontroller looks at P1.1. If P1.1 is not high, microcontroller decides this is not a clap and goes back to monitor P1.0, if P1.1 is high, microcontroller starts timer0 and monitors P1.1. If P1.1 does not go low within 65.53ms, microcontroller decides this is not a clap, and starts monitoring P1.0 again.
If P1.1 does go to 0 within 65.53ms, microcontroller looks at time periods for which P1.0 was high, and P1.1 was high, if these times lie within a certain range, a clap is registered, otherwise not.
If the clap registered is the first clap, timer1 starts, and microcontroller goes back to monitor P1.0, if the clap registered is the second clap, interclap time is calculated, and according to the value found, corresopnding LED is made to blink. The maximum interclap delay is slightly larger than 5s, after that, the first clap is discarded and microcontroller starts to monitor P1.0.

interclap duration	LED which blinks
1s - 2s	P1.4
2s - 3s	P1.5
3s - 4s	P1.6
4s - 5s	P1.7

Table 2: Interclap durations and corresponding LEDs

6 Bill Of Materials for clap detector

The bill of materials for the components required is given below. In the following we have excluded the cost of 8051 micro-controller kit (AT89C51).

Quantity	References from Schematics	Value	Unit cost
4 Capacitors			
2	C_{env},C_{pk}	1 μF	₹79.00
1	C_{fm}	0.82 μF	₹50.00
1	C_{fn}	2.2 μF	₹20.00
Sub-total:			₹228.00
26 Resistors			
4	$R_{d,1}$ to $R_{d,4}$	1 $k\Omega$	₹0.30
2	R_b	2 $k\Omega$	₹0.30
6	$R_{env,1}$; $R_{pk,1}$; $R_{p,1}$; $R_{p,3}$; $R_{p,5}$; $R_{n,2}$	10 $k\Omega$	₹0.30
1	R_1	15 $k\Omega$	₹0.30
7	R_g; $R_{p,1}$; $R_{p,3}$; $R_{p,5}$	20 $k\Omega$	₹0.30
1	R_2	75 $k\Omega$	₹0.30
1	R_1	160 $k\Omega$	₹0.30
1	R_{env}	168 $k\Omega$	₹0.30
1	R_g	240 $k\Omega$	₹0.30
1	$R_{n,1}$	470 $k\Omega$	₹0.30
1	R_{pk}	510 $k\Omega$	₹0.30
Sub-total:			₹13.00
6 Integrated Circuits			
4	U_{ref}; U_a; $U_{env,1}$; $U_{env,2}$; $U_{pk,1}$; $U_{pk,2}$; $U_{b,1}$ to $U_{b,4}$; $U_{c,1}$ to $U_{c,3}$; U_n	LM324	₹30.00
1	X_1; X_2	74HC86	₹49.00
1	A_1; A_2	7408	₹49.00
Sub-total:			₹218.00
4 Diodes			
4	$D_{env,1}$; $D_{env,2}$; $D_{pk,1}$; $D_{pk,2}$	1N4007	₹3.50
Sub-total			₹14.00
1 Miscellaneous			
1	Electret Microphone	CMA-4544PF-W	₹60.00
Subtotal:			₹60.00
Grand Total:			₹533.00

Table 3: Bill of Materials

References

[1] *How Electret Microphones Work – Full Tutorial and Diagram.* `https://www.homemade-circuits.com/how-electret-microphone-works/`

[2] *CMA-4544PF-W Datasheet - Electret Condenser Microphones.* CUI Devices, January 2020.

[3] John Caldwell. *Single-Supply, Electret Microphone Pre-Amplifier Reference Design.* Texas Instruments, January 2015.

[4] *Precision Rectifier Circuits* `https://www.site.uottawa.ca/r̃habash/ELG4135L8.pdf`.

[5] *LMx24-N, LM2902-N Low-Power, Quad-Operational Amplifiers.* Texas Instruments, Rev. ed. January 2015.

[6] Kashinath Murmu and Ravi Sonkar. *Control of Light and Fan with Whistle and Clap Sounds.* Department of Electrical Engineering, IIT Bombay, November 2004

[7] *SN54HC86, SN74HC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES.* Texas Instruments, Rev. ed. August 2003.

[8] *SN5408, SN54LS08, SN54S08 SN7408, SN74LS08, SN74S08 QUADRUPLE 2-INPUT POSITIVE-AND GATES.* Texas Instruments, Rev. ed. March 1988.

A Link to Data files and Codes

1. Link to C code file:
   https://github.com/Adbhut-Vipin-Bhardwaj/EDL_microcontroller_code/blob/main/code/main.c
2. Link to audio files used:
   https://drive.google.com/drive/folders/1nwC-QD1foV8RV8hzZ46WMPKoWpBcISiE?usp=sharing